IDEC Chip Design Contest

MV – HEVC Chip Design using Memory & Delay Control Circuit

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ABSTRACT

- This MPW Chip design for MV-HEVC decoder using wide band data rate. As a video processor, HEVC is a standard in mobile and other industry. Multiview also require in sports area. However, the video data is pretty generous size and it need a high-speed interface from camera to processor.

- We designed IO pad with delay cells to resolve the timing issue. In addition, internal registers were controlled using I2C block and external memory controllers are designed due to lack of internal memory capacity. The implementation of the algorithm made the chip through **the Samsung 65nm foundry process**.

BACKGROUND

MV - HEVC

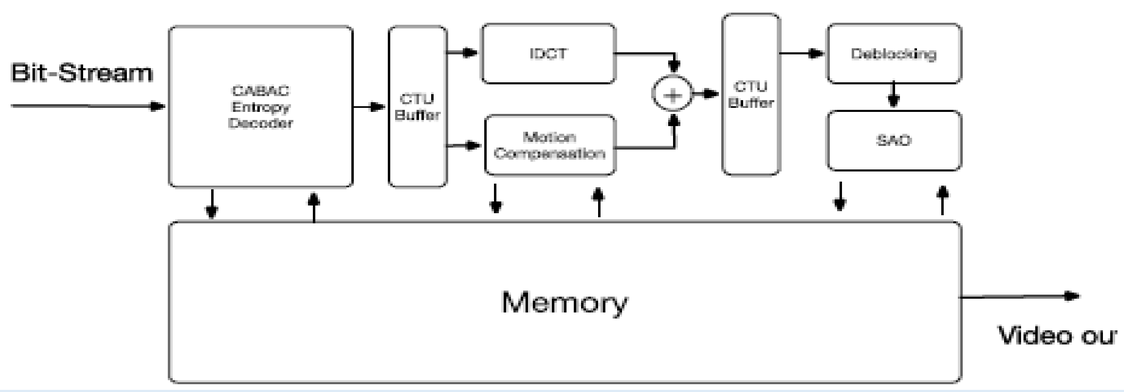

Fig. 1 MV – HEVC Block Diagram

- When the image data enters the bit-stream, it is processed through the entropy Decoder and then buffered again before processing IDCT, Motion Composition. The image data processed in such a way is eventually restored via Deblocking and SAO. High capacity memory is essential for intermediate storage of image data here.

Delay Control Unit

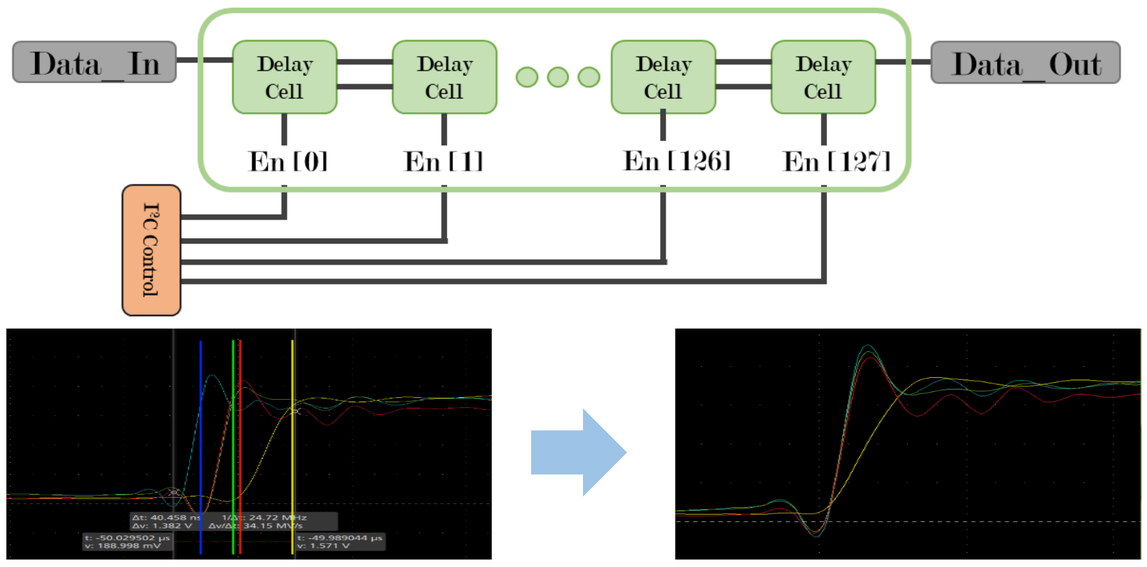

Fig. 2 Delay Cell Block Diagram & Simulation

- **Delay cell** was added as shown in Figure to solve the timing violation, which can occur even in the same data input in real chip operation. This can be controlled using a total of 128 layers and adjusted up to 40 ns.

- In this Chip, **I2C Slave** were designed inside simultaneously to control registers that required initial setting and monitor the condition of the chip according to the situation.

CHIP DIAGRAM

CHIP-DIAGRAM

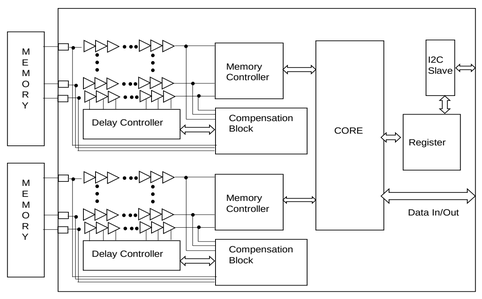

Fig. 4. Chip Block Diagram

- Setting the initial decoding register using I2C
- Input Data Timing arrange Using Delay Cell
- MV-HEVC Decoding & Load external memory
- Check Output Data
- Output Data Timing arrange with Delay Cell

Test Environment

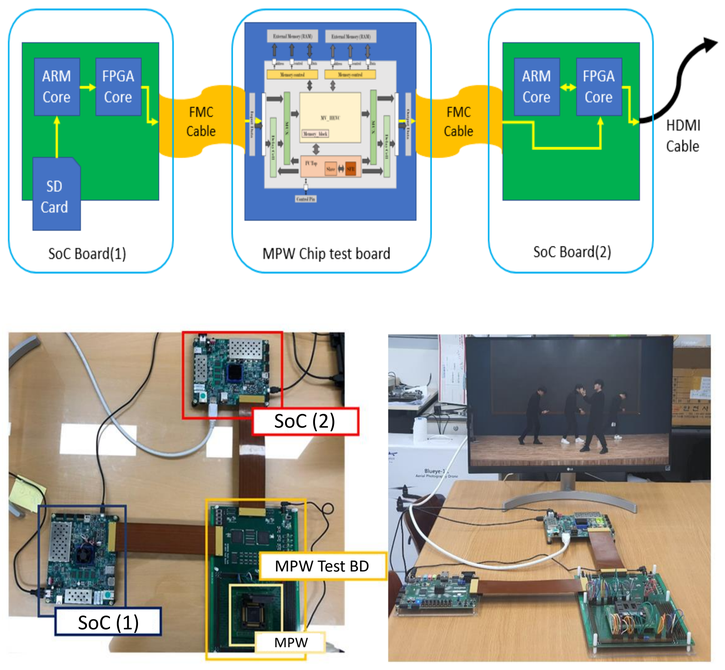

Fig. 4. Test Diagram & Test Environment

1. Perform the required initial setup between decoding using i2c on the soc board (1).
2. Use FMC cable to send an encoding image stored in the SD card.
3. Process all decoding operations inside the chip & load external memory
4. Output the decoded image data as a chip from the soc board (2), in HDMI.

RESULT

Table 1 Delay Cell Size

Unit	Synthesis	Place & Route
Unit Delay cell	10.24 um^2	13.312 um^2
Memory Control	276.48 um^2	365.23 um^2
Delay Control	792.32 um^2	117.1712 um^2

Table 2 compare delay step

This work	This Work	[4]
Process	65 nm	130 nm
Period	200 ps	340 ps

Table 3 Read/Write Time

Unit	clk	1 time	16bit/16MB	16bit/32MB
Read	4	200 ns	2 s	4 s
Write	5	250 ns	1.6 s	3.2 s

Fig. 4.1. Delay Cell & Memory Control Table

Table 4 Operation Power

Unit	Power
Core Power	4.0738 mW
Leakage Power	0.6719 mW

Fig. 4.2. Chip Operation Power

• PIPP, 640x480

Sequence	QP	Bit-rate (kbps)	FPS
Our sequence 640 x 480	25	2558.52	36.73
	30	1241.94	40.55
	35	547.78	42.97
	40	297.73	46.12

• PIPP, 1024 X 768

Sequence	QP	Bit-rate (kbps)	FPS
Balloons 1024 x 768	25	4861.2	12.28
	30	2359.7	14.5
	35	1040.8	15.57
	40	565.7	17.63
Kendo 1024 x 768	25	1462.7	13.23
	30	643.9	15.13
	35	350.2	16.89
	40	207.3	18.28
Newspaper 1024 x 768	25	3246.0	15.97
	30	1232.7	17.63
	35	590.4	18.68
	40	307.8	20.05

Fig. 4.3. Resolution Table

CONCLUSION

- Due to the nature of video processing, many of the memory was used, and many of the constraints were followed, so we tried to solve this problem by using external memory. However, due to limitations in operating frequency of external memory, real-time computational processing with high resolution was somewhat difficult as it fell from the originally intended operating speed. Therefore, the process of amending and supplementing this part is necessary.

ACKNOWLEDGE

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